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EXAMINER	
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ART UNIT	PAPER NUMBER
2827	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Application No.	Applicant(s)	
09/190,378	ALBERT, DOUGLAS M.	
Examiner	**Art Unit**	
David E Graybill	2827	

Office Action Summary

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24 and 28-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12* is/are allowed.

6)☒ Claim(s) *1-12,14-24 and 28-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other. .

The response filed 3-22-2 is non-responsive to the Office action filed 4-20-1 because it fails to conform to the provisions of MPEP 714.03:

> 714.03 Amendments Not Fully Responsive - Action To Be Taken: Where a bona fide response to an examiner's action is filed before the expiration of a permissible period, but through an apparent oversight or inadvertence some point necessary to a complete response has been omitted - such as an amendment or argument as to one or two of several claims involved or signature to the amendment - the examiner, as soon as he or she notes the omission, should require the applicant to complete his or her response within a specified time limit (usually one month) if the period for response has already expired or insufficient time is left to take action before the expiration of the period. If this is done the application should not be held abandoned even though the prescribed period has expired.

Specifically, the response is incomplete because applicant has not affirmed the oral election of Group I, claims 1-24 and 28-32, as required.

Because the response appears to be bona fide, but through an apparent oversight or inadvertence the response is incomplete, and in order to continue to afford applicant the benefit of compact prosecution, the requirement to complete the response within a one month time limit is waived, the amendment is entered, and the claims are examined on the merits.

The declaration filed on 3-22-2 under 37 CFR 1.131 is sufficient to overcome the Riding reference.

The indicated allowability of claims 17-19 is withdrawn in view of the newly discovered and applied Schneider reference. Rejections based on the newly cited reference follow.

Claims 28-32 of this application have been copied by applicant from U.S. Patent No. 5,888,883. These claims are not patentable to applicant because they are anticipated by and unpatentable over the prior art applied supra.

An interference cannot be initiated since a prerequisite for interference under 37 CFR 1.606 is that the claim be patentable to applicant subject to a judgment in the interference.

In the rejections infra, reference labels are generally recited only for the first recitation of identical claim language.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 4, 5, 7-10, 13, 14, 17, 18 and 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Tanaka and Poole.

As cited supra, Tanaka teaches the following:

1. A method for manufacturing a plurality dies containing thinned integrated circuits from a semiconductor wafer having a thickness, a front surface and a backside surface, comprising: defining a plurality of grooves into said front surface of said

semiconductor wafer to define said plurality of dies, said grooves penetrating into said surface at a predetermined distance less than said thickness of said semiconductor wafer so that said plurality of dies remain integral with said wafer; mounting said wafer to a flat substrate 2 to support said wafer, said wafer being mounted to said substrate with said front surface turned toward said substrate; mechanically removing a predetermined portion of said backside of said wafer until said thickness of said wafer is reduced to expose said plurality of grooves to said backside in preparation to separating said plurality of said dies, said dies remaining mounted to said substrate; and releasing said plurality of dies from said substrate.

10. The method of 1 wherein mounting said wafer to said flat substrate comprises affixing said wafer by means of an adhesive.

13. The method of 1 further comprising mounting a die from said plurality of dies onto a flexible film 2.

14. The method of 13 further comprising sealing said die mounted on said flexible film.

17. The method of 1 where mounting said wafer to said substrate comprises affixing said front surface of said wafer to substrate on a surface of said substrate provided with a

plurality of grooves defined in said substrate to facilitate the flow of material across said surface of said substrate between said surface of said substrate and said front surface of said wafer.

18. The method of 17 wherein affixing said front surface to said flat substrate comprises affixing said front surface using an adhesive material disposed between said front surface and said flat substrate.

20. The method of 1 where mechanically removing said wafer comprises grinding said backside portion of said wafer with at least one cycle of a predetermined grinding advance rate followed by a nonadvancing dwell.

21. The method of 20 where grinding with a least one advance rate and dwell comprises at least one reduction in said advance rate.

23. The method of 1 where defining said plurality of grooves in said front surface of said wafer comprises defining linear grooves into said front surface of said wafer in an intersecting grid pattern to define each of said plurality of dies, thereby isolating each die by a surrounding moat of stress relieving grooves.

To further clarify the teaching of the limitation "to facilitate the flow of material across said surface of said

substrate between said surface of said substrate and said front surface of said wafer," it is noted that this limitation is merely a statement of intended use which does not result in a manipulative difference as compared to the process of Tanaka. Furthermore, because the process of Tanaka is inherently capable of being used for the same intended use, the statement of intended use does not patentably distinguish the claimed process from the process of Tanaka.

To further clarify the teaching of a process where mechanically removing the wafer comprises grinding the backside portion of the wafer with at least one cycle of a predetermined grinding advance rate followed by a nonadvancing dwell, and where grinding with at least one advance rate and dwell comprises at least one reduction in the advance rate, it is noted that these limitations are inherent in the process of grinding and stopping grinding of Tanaka.

However, Tanaka does not appear to explicitly teach a rigid substrate or the following:

4. The method of 1 where mounting said flat substrate to said front surface of said wafer comprises affixing an optically flat substrate to said front surface of said wafer.

5. The method of 4 where affixing said optically flat substrate comprises affixing said front surface of said wafer to

a surface of said substrate which has vertical variations of approximately one micron or less across said surface.

Nonetheless, at column 3, lines 26-47, column 4, lines 46-50, column 5, line 52 to column 6, line 63, and column 7, line 51 to column 8, line 8, Poole teaches a process wherein affixing an optically flat substrate comprises affixing a front surface of a wafer shaped substrate to a surface of a rigid substrate which has vertical variations of approximately one micron or less across said surface ("a flatness tolerance of $\lambda/2$ or better, as measured on a 1/10 wave optical flat using a monochromatic helium light source"). Furthermore, it would have been obvious to combine the process of Poole with the process of Tanaka because it would facilitate manufacture of thin circuits.

Also, the combination of Tanaka and Poole does not appear to explicitly teach the following:

7. The method of 1 wherein defining said plurality of said grooves in said wafer comprises defining grooves approximately 50 microns deep into said front surface of said wafer.

8. The method of 7 wherein mechanically removing a portion of said wafer removes said backside portion of said wafer until said wafer has a thickness of 50 microns or less.

9. The method of 8 wherein mechanically removing a portion of said wafer removes said backside portion of said wafer until said wafer has a thickness of approximately 25 microns or less.

Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

In addition, Tanaka and Poole do not appear to explicitly teach the following:

22. The method of 21 further comprising polishing said thinned backside surface of said wafer by a dry chemical etch having an etch rate of less than one micron per minute or a mechanical polish having an advance rate of less than one micron per minute.

Regardless, Tanaka and Poole teach mechanical polishing having an inherent advance rate, and the particular claimed advance rate would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization because applicant has not disclosed that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another rate. Moreover, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. Indeed, at page 12, lines 7-11, applicant explicitly discloses that the particular claimed advance rate is determined by manufacturing constraints such as the particular type of wafer grinder.

Claims 6 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Tanaka and Poole as

applied to claims 1, 4, 5, 7-10, 13, 14, 17, 18 and 20-23, and further in combination with Fu (5807787).

The combination of Tanaka and Poole does not appear to explicitly teach the following:

6. The method of 1 further comprising disposing a polyimide layer on said front surface before said grooves are defined therein and prior to mounting to said flat substrate, so that said polyimide layer absorbs stress induced into said wafer when mechanically removing a portion of said wafer.

11. The method of 10 further comprising disposing a polyimide layer on said front surface before said grooves are defined therein and prior to affixing to said flat substrate, so that said polyimide layer absorbs stress induced into said wafer when said grooves are mechanically formed in said wafer.

Notwithstanding, at column 1, lines 16-45, Fu teaches this process. Moreover, it would have been obvious to combine the process of Fu with the process of the applied prior art because it would absorb stress induced into the wafer when the grooves are mechanically formed in the wafer.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka and Poole as applied to claims 1, 4, 5, 7-10, 13, 14, 17, 18 and 20-23, and further in combination with Clifton.

Tanaka and Poole do not appear to explicitly teach the following:

15. The method of 13 where mounting said die on said flexible film further comprises electrically coupling an integrated circuit in said die to metalizations provided on said film.

Regardless, at column 5, lines 51-67, Clifton teaches mounting a die 415 on a flexible film 426 comprising electrically coupling an integrated circuit in the die to metalizations 421 provided on the film. Furthermore, it would have been obvious to combine the process of Clifton with the process of Tanaka and Poole because it would facilitate smart card fabrication.

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Tanaka, Poole and Clifton as applied to claim 15, and further in combination with Hayes (5681757).

The combination of Tanaka, Poole and Clifton does not appear to explicitly teach the following:

16. The method of 15 where electrically coupling said integrated circuit on said die to metalizations on said film comprises disposing said die with said front surface in contact

with said metalizations on said film and coupled thereto by means of conductive epoxy.

Still, at column 10, lines 38-53, Hayes teaches a process where electrically coupling an integrated circuit on a die 96 to metalizations 86 on a substrate comprises disposing the die with a front surface in contact with the metalizations on the substrate and coupled thereto by means of conductive epoxy 92. Also, it would have been obvious to combine the process of Hayes with the process of the combination of applied prior art because it would facilitate electrical coupling of the die.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka and Poole as applied to claims 1, 4, 5, 7-10, 13, 14, 17, 18 and 20-23, and further in combination with Ishiwata (5300172).

Tanaka and Poole do not appear to explicitly teach the following:

19. The method of 18 further comprising pressing said wafer and substrate together with said adhesive material therebetween and curing said adhesive material.

Yet, at column 8, lines 8-21, Ishiwata teaches pressing a wafer and substrate together with an adhesive material therebetween and curing ["semi-cure"] said adhesive material. Furthermore, it would have been obvious to combine the process

of Ishiwata with the process of Tanaka and Poole because it would provide an adhesive material.

Although Tanaka and Poole do not appear to explicitly teach curing the adhesive material while maintaining the pressure between the wafer and substrate, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed process sequence because applicant has not disclosed that the limitation is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical. Moreover, it is well established that, in a well known process, the order of performing process steps is prima facie obvious in the absence of new or unexpected results. Ex parte Rubin 128 USPQ (PO BdPatApp 1959).

Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka and Poole as applied to claims 1, 4, 5, 7-10, 13, 14, 17, 18 and 20-23, and further in combination with Cronin (5925924).

Tanaka and Poole do not appear to explicitly teach the following:

24. The method of 1 further comprising stacking a plurality of dies manufactured by said method, and electrically interconnecting said plurality of dies.

Nonetheless, at column 10, lines 9-28, Cronin teaches this process. Moreover, it would have been obvious to combine the process of Cronin with the process of Tanaka and Poole because it would facilitate stacked package manufacture.

Claims 1, 3, 10, 17, 18, 20, 21 and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Schneider (4023260).

At column 3, line 36 to column 5, line 46, Schneider teaches the following:

1. A method for manufacturing a plurality dies containing thinned integrated circuits from a semiconductor wafer having a thickness, a front surface and a backside surface, comprising: defining a plurality of grooves ["notches'] into said front surface of said semiconductor wafer to define said plurality of dies, said grooves penetrating into said surface at a predetermined distance less than said thickness of said semiconductor wafer so that said plurality of dies remain integral with said wafer; mounting said wafer to a flat rigid substrate ["lapping block"] to support said wafer, said wafer being mounted to said substrate with said front surface turned toward said substrate; mechanically removing a predetermined

portion of said backside of said wafer until said thickness of said wafer is reduced to expose said plurality of grooves to said backside in preparation to separating said plurality of said dies, said dies remaining mounted to said substrate; and releasing said plurality of dies from said substrate.

3. The method of 1 further comprising disposing a layer of material 202 on said front surface of said wafer before defining said plurality of grooves into said front surface of said wafer.

10. The method of 1 wherein mounting said wafer to said flat substrate comprises affixing said wafer by means of an adhesive ["paraffin or wax as the adhesive"].

17. The method of 1 where mounting said wafer to said substrate comprises affixing said front surface of said wafer to substrate on a surface of said substrate provided with a plurality of grooves defined in said substrate to facilitate the flow of material across said surface of said substrate between said surface of said substrate and said front surface of said wafer.

18. The method of 17 wherein affixing said front surface to said flat substrate comprises affixing said front surface using an adhesive material disposed between said front surface and said flat substrate.

20. The method of 1 where mechanically removing said wafer comprises grinding said backside portion of said wafer with at least one cycle of a predetermined grinding advance rate followed by a nonadvancing dwell.

21. The method of 20 where grinding with a least one advance rate and dwell comprises at least one reduction in said advance rate.

23. The method of 1 where defining said plurality of grooves in said front surface of said wafer comprises defining linear grooves into said front surface of said wafer in an intersecting grid pattern to define each of said plurality of dies, thereby isolating each die by a surrounding moat of stress relieving grooves.

To further clarify the teaching of the limitation "to facilitate the flow of material across said surface of said substrate between said surface of said substrate and said front surface of said wafer," it is noted that this limitation is merely a statement of intended use which does not result in a manipulative difference as compared to the process of Schneider. Furthermore, because the process of Schneider is inherently capable of being used for the same intended use, the statement of intended use does not patentably distinguish the claimed process from the process of Schneider.

To further clarify the teaching of a process where mechanically removing the wafer comprises grinding the backside portion of the wafer with at least one cycle of a predetermined grinding advance rate followed by a nonadvancing dwell, and where grinding with at least one advance rate and dwell comprises at least one reduction in the advance rate, it is noted that these limitations are inherent in the process of grinding and stopping grinding of Schneider.

To further clarify the teaching of stress relieving grooves, this limitation is an inherent property of the grooves of Schneider.

Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider as applied to claims 1, 3, 10, 17, 18, 20, 21 and 23, and further in combination with Poole (5162251).

Schneider does not appear to explicitly teach the following:

4. The method of 1 where mounting said flat substrate to said front surface of said wafer comprises affixing an optically flat substrate to said front surface of said wafer.

5. The method of 4 where affixing said optically flat substrate comprises affixing said front surface of said wafer to

a surface of said substrate which has vertical variations of approximately one micron or less across said surface.

Nonetheless, at column 3, lines 26-47, column 4, lines 46-50, column 5, line 52 to column 6, line 63, and column 7, line 51 to column 8, line 8, Poole teaches a process wherein affixing an optically flat substrate comprises affixing a front surface of a wafer shaped substrate to a surface of a rigid substrate which has vertical variations of approximately one micron or less across said surface ("a flatness tolerance of $\lambda/2$ or better, as measured on a 1/10 wave optical flat using a monochromatic helium light source"). Furthermore, it would have been obvious to combine the process of Poole with the process of Schneider because it would facilitate the step of removing a portion of the backside of the wafer of Schneider.

Claims 2, 7-9, 19 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider as applied to claims 1, 3, 10, 17, 18, 20, 21 and 23.

As cited, Schneider teaches the following:

2. The method of 1 further comprising disposing a planarizing layer of material ["paraffin or wax as the adhesive"] on said front surface of said wafer into which said plurality of grooves have been defined.

However, Schneider does not appear to explicitly teach disposing the material prior to mounting said front surface of said wafer to said flat substrate.

Nonetheless, the material is present when the front surface is mounted to the substrate, and it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed disposing sequence because applicant has not disclosed that the limitation is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical. Moreover, it is well established that, in a well known process, the order of performing process steps is prima facie obvious in the absence of new or unexpected results. Ex parte Rubin 128 USPQ (PO BdPatApp 1959).

Also, Schneider does not appear to explicitly teach the following:

7. The method of 1 wherein defining said plurality of said grooves in said wafer comprises defining grooves approximately 50 microns deep into said front surface of said wafer.

8. The method of 7 wherein mechanically removing a portion of said wafer removes said backside portion of said wafer until said wafer has a thickness of 50 microns or less.

9. The method of 8 wherein mechanically removing a portion of said wafer removes said backside portion of said wafer until said wafer has a thickness of approximately 25 microns or less.

Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

In addition, Schneider teaches the following:

19. The method of 18 further comprising pressing said wafer and substrate together with said adhesive material therebetween and curing said adhesive material.

To further clarify the teaching of curing the adhesive material, it is noted that it is inherent that the wax becomes solid or thickened by chemical or physical alteration; therefore it is set and cured.

Although Schneider does not appear to explicitly teach curing the adhesive material while maintaining the pressure between the wafer and substrate, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed process sequence because applicant has not disclosed that the limitation is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical. Moreover, it is well established that, in a well known process, the order of performing process steps is prima facie obvious in the absence of new or unexpected results. Ex parte Rubin 128 USPQ (PO BdPatApp 1959).

Schneider also does not appear to explicitly teach the following:

22. The method of 21 further comprising polishing said thinned backside surface of said wafer by a dry chemical etch

having an etch rate of less than one micron per minute or a mechanical polish having an advance rate of less than one micron per minute.

Regardless, Schneider teaches mechanical polishing having an inherent advance rate, and the particular claimed advance rate would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization because applicant has not disclosed that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another rate. Moreover, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. Indeed, at page 12, lines 7-11, applicant explicitly discloses that the particular claimed advance rate is determined by manufacturing constraints such as the particular type of wafer grinder.

Claims 6 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider as applied to claims 1, 3, 10, 17, 18, 20, 21 and 23, and further in combination with Fu (5807787).

Schneider does not appear to explicitly teach the following:

6. The method of 1 further comprising disposing a polyimide layer on said front surface before said grooves are defined therein and prior to mounting to said flat substrate, so that said polyimide layer absorbs stress induced into said wafer when mechanically removing a portion of said wafer.

11. The method of 10 further comprising disposing a polyimide layer on said front surface before said grooves are defined therein and prior to affixing to said flat substrate, so that said polyimide layer absorbs stress induced into said wafer when said grooves are mechanically formed in said wafer.

Notwithstanding, at column 1, lines 16-45, Fu teaches this process. Moreover, it would have been obvious to combine the process of Fu with the process of Schneider because it would absorb stress induced into the wafer when the grooves are mechanically formed in the wafer.

Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider as applied to claims 1, 3, 10, 17, 18, 20, 21 and 23, and further in combination with Clifton.

Schneider does not appear to explicitly teach the following:

13. The method of 1 further comprising mounting a die from said plurality of dies onto a flexible film.

14. The method of 13 further comprising sealing said die mounted on said flexible film.

15. The method of 13 where mounting said die on said flexible film further comprises electrically coupling an integrated circuit in said die to metalizations provided on said film.

Regardless, as cited supra, Clifton teaches mounting a die 415 on a flexible film 426, sealing a die 415 mounted on a flexible film comprising electrically coupling an integrated circuit in the die to metalizations 421 provided on the film. Furthermore, it would have been obvious to combine the process of Clifton with the process of Schneider because it would facilitate smart card fabrication.

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Schneider and Clifton as applied to claims 13-15, and further in combination with Hayes (5681757).

The combination of Schneider and Clifton does not appear to explicitly teach the following:

16. The method of 15 where electrically coupling said integrated circuit on said die to metalizations on said film

comprises disposing said die with said front surface in contact with said metalizations on said film and coupled thereto by means of conductive epoxy.

Still, at column 10, lines 38-53, Hayes teaches a process where electrically coupling an integrated circuit on a die 96 to metalizations 86 on a substrate comprises disposing the die with a front surface in contact with the metalizations on the substrate and coupled thereto by means of conductive epoxy 92. Also, it would have been obvious to combine the process of Hayes with the process of the combination of applied prior art because it would facilitate electrical coupling of the die.

Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider as applied to claims flexible film, and further in combination with Cronin (5925924).

Schneider does not appear to explicitly teach the following:

24. The method of 1 further comprising stacking a plurality of dies manufactured by said method, and electrically interconnecting said plurality of dies.

Nonetheless, at column 10, lines 9-28, Cronin teaches this process. Moreover, it would have been obvious to combine the process of Cronin with the process of Schneider because it would facilitate stacked package manufacture.

Claims 28-30 are rejected under 35 U.S.C. 102(b) as anticipated by Tanaka (JP5-74934) or, in the alternative, under 35 U.S.C. 103(a) as obvious over the combination of Tanaka (JP5-74934) and Poole (5162251).

In the English translations and figures, Tanaka teaches the following:

28. A wafer dividing method comprising the steps of: forming grooves 12 in a surface 1a of a wafer 1, on which surface semiconductor elements 11 are formed, along dicing lines ["street"], said grooves being deeper than a thickness of a finished chip 13; attaching a holding member 2 on said surface of the wafer on which the semiconductor elements are formed; and lapping and polishing a bottom surface 1b of the wafer to said thickness of the finished chip, thereby dividing the wafer into chips, wherein in the step of dividing the wafer into the chips, the lapping and polishing is continued until the thickness of the wafer becomes equal to the thickness of the finished chip, even after the wafer has been divided into the chips by the lapping and polishing.

29. The wafer dividing method according to 28 wherein a depth of each groove is greater than the thickness of the finished chip by at least 5 μm.

30. The wafer dividing method according to 28 wherein said holding member comprises a substrate coated with an adhesive material ["resin pressure sensitive adhesive sheet"].

Although Tanaka does not appear to literally teach the instantly claimed "lapping" and "polishing," Tanaka explicitly teaches "grinding," and grinding is inherently both lapping and polishing. Indeed, although applicant provides no literal support in the original disclosure for the term *lapping*, at page 9, lines 21-26 of the "Request For Interference With a Patent" applicant cites the original specification at page 11, line 20 to page 12, line 1, as support for the term *lapping*, wherein applicant teaches that grinding is inherently both lapping and polishing. Similarly, applicant also supports the premise that grinding is lapping and polishing at page 5, lines 8-14, page 7, lines 17-19, and page 8, lines 9-13.

In any case, in the alternative, at column 3, lines 25-34 and 42-46, column 4, lines 46-50, column 5, line 52 to column 6, line 64, column 7, lines 10-14, and column 7, line 51 to column 8, line 8, Poole teaches literally a process of lapping and polishing a silicon substrate. Moreover, it would have been obvious to combine the process of Poole with the process of Tanaka because it would enable the grinding of Tanaka.

Claims 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka or Tanaka and Poole as applied to claims 28-30, and further in combination with Clifton (5480842).

As cited, Tanaka or the combination of Tanaka and Poole teach the following:

31. A method of manufacturing a semiconductor device, comprising the steps of: forming semiconductor elements in a major surface of a wafer; forming grooves in said major surface of the wafer along dicing lines, said grooves being deeper than a thickness of a finished chip; attaching an adhesive sheet 2 on said major surface of the wafer; lapping and polishing a bottom surface of the wafer to said thickness of the finished chip, thereby dividing the wafer into chips; and separating each of the divided chips from the adhesive sheet, wherein in the step of dividing the wafer into the chips, the lapping and polishing is continued until the thickness of the wafer becomes equal to the thickness of the finished chip, even after the wafer has been divided into the chips by the lapping and polishing.

32. The method of manufacturing a semiconductor device, according to 31, wherein a depth of each groove is greater than the thickness of the finished chip by at least 5 μm.

However, neither Tanaka nor Tanaka and Poole appear to teach sealing each chip in a package.

Nevertheless, as cited supra, Clifton teaches sealing each chip 20 in a package. Furthermore, it would have been obvious to combine the process of Clifton with the process of the applied prior art because it would facilitate smart card fabrication.

Claim 12 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Applicant's remarks filed 3-22-2 have been fully considered and are adequately addressed in the rejection supra.

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions similar to the instant invention.

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to Group 2800 Customer Service whose telephone number is 703-306-3329.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (703) 308-2947. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

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17-Nov-02